CLAIMS:

1. A processing device comprising:

one or more resources;

a plurality of peripheral bus interfaces operably coupled to the one or more resources and couple able to a peripheral bus fabric to support resource sharing with a plurality of other processing devices;

primary routing resources programmable with a plurality of address ranges, the processing device operable to determine a routing of peripheral bus transactions among the plurality of peripheral bus interfaces based upon a destination address of the peripheral bus transaction and primary routing resources contents; and

a node ID register programmable with a plurality of override indications, the processing device operable to determine an override routing of peripheral bus transactions among the plurality of peripheral bus interfaces based upon a destination node ID of the peripheral bus transaction and node ID register contents.

2. The processing device of claim 1 wherein the processing device determines the node ID of the destination processing device based upon a set of most significant bits of the destination address of the peripheral bus transaction.

3. The processing device of claim 1 wherein the processing device may ignore the override routing based upon node ID register contents.

4. The processing device of claim 1 wherein the override routing applies to cache coherency peripheral bus transactions.

5. The processing device of claim 1 wherein the override routing applies to input/output peripheral bus transactions.

6. The processing device of claim 1 wherein the override routing applies to both cache coherency peripheral bus transactions and to input/output peripheral bus transactions.

7. The processing device of claim 6, wherein the override routing is selectively disable able with regard to cache coherency peripheral bus transactions and/or to input/output peripheral bus transactions.

8. The processing device of claim 6 wherein the override routing does not apply to packet data peripheral bus transactions.

9. The processing device of claim 1, wherein:

the override routing relates to one of the plurality of peripheral bus interfaces;

the override routing indicates to route the peripheral bus transaction to either a primary port of the peripheral bus interface or to a secondary port of the peripheral bus interface.

10. The processing device of claim 1 wherein the node ID register comprises an entry for each of a plurality of represented processing devices, each entry comprising:

a node ID;

an override bit corresponding to input/output peripheral bus transactions;

a primary/secondary indication corresponding to input/output peripheral bus transactions;

an override bit corresponding to cache coherency peripheral bus transactions; and

a primary/secondary indication corresponding to cache coherency peripheral bus transactions.

11. The processing device of claim 1 further comprising:

a virtual peripheral bus operably coupled to each of the plurality of peripheral bus interfaces; and

an emulated configurable host bridge operably coupled to the virtual peripheral bus.

12. The processing device of claim 11, wherein at least one of the peripheral bus interfaces is programmable so that either its primary port or its secondary port is operably coupled to the virtual peripheral bus.

13. The processing device of claim 12, wherein the override routing identifies either a primary port or a secondary port of a programmable one of the peripheral bus interfaces.

14. A processing device comprising:

a processor;

memory;

a virtual peripheral bus operably coupled to the processor and to the memory;

a plurality of peripheral bus interfaces operably coupled to the virtual peripheral bus and couple able to a peripheral bus fabric to support resource sharing with a plurality of other processing devices;

primary routing resources programmable with a plurality of address ranges, the processing device operable to determine a routing of peripheral bus transactions among the plurality of peripheral bus interfaces based upon a destination address of the peripheral bus transaction and primary routing resources contents; and

a node ID register programmable with a plurality of override indications, the processing device operable to determine an override routing of peripheral bus transactions among the plurality of peripheral bus interfaces based upon a destination node ID of the peripheral bus transaction and node ID register contents.

15. The processing device of claim 14, wherein:

the virtual peripheral bus is emulated by the processing device; and

the plurality of peripheral bus interfaces operably couple to the processor and memory via a system bus.

16. The processing device of claim 14, wherein:

the virtual peripheral bus is emulated by the processing device; and

the plurality of peripheral bus interfaces operably couple to the processor and memory via a system bus and at least one other coupling device.

17. The processing device of claim 15, wherein the at least one other coupling device is selected from the group consisting of switches, packet managers, and node controllers.

18. The processing device of claim 14 wherein the processing device determines the node ID of the destination processing device based upon a set of most significant bits of the destination address of the peripheral bus transaction.

19. The processing device of claim 14 wherein the processing device may ignore the override routing based upon node ID register contents.

20. The processing device of claim 14 wherein the override routing applies to cache coherency peripheral bus transactions.

21. The processing device of claim 14 wherein the override routing applies to input/output peripheral bus transactions.

22. The processing device of claim 14 wherein the override routing applies to both cache coherency peripheral bus transactions and to input/output peripheral bus transactions.

23. The processing device of claim 22, wherein the override routing is selectively disable able with regard to cache coherency peripheral bus transactions and/or to input/output peripheral bus transactions.

24. The processing device of claim 22 wherein the override routing does not apply to packet data peripheral bus transactions.

25. The processing device of claim 14, wherein:

the override routing relates to one of the plurality of peripheral bus interfaces;

the override routing indicates to route the peripheral bus transaction to either a primary port of the peripheral bus interface or to a secondary port of the peripheral bus interface.

26. The processing device of claim 14 wherein the node ID register comprises an entry for each of a plurality of represented processing devices, each entry comprising:

a node ID;

an override bit corresponding to input/output peripheral bus transactions;

a primary/secondary indication corresponding to input/output peripheral bus transactions;

an override bit corresponding to cache coherency peripheral bus transactions; and

a primary/secondary indication corresponding to cache coherency peripheral bus transactions.

27. The processing device of claim 14 further comprising:

a virtual peripheral bus operably coupled to each of the plurality of peripheral bus interfaces; and

an emulated configurable host bridge operably coupled to the virtual peripheral bus.

28. The processing device of claim 27, wherein at least one of the peripheral bus interfaces is programmable so that either its primary port or its secondary port is operably coupled to the virtual peripheral bus.

29. A method for operating a processing device having one or more resources and a plurality of peripheral bus interfaces that are operable to couple the one or more resources to one or more other processing devices via a peripheral bus fabric, the method comprising:

receiving a peripheral bus transaction at the processing device;

determining a primary routing of the peripheral bus transaction among the plurality of peripheral bus interfaces based upon a destination address of the peripheral bus transaction and primary routing resources contents;

determining an override routing of peripheral bus transactions among the plurality of peripheral bus interfaces based upon a destination node ID of the peripheral bus transaction and node ID register contents; and

routing the peripheral bus transaction among the plurality of peripheral bus interfaces according to one of the primary routing and the override routing.

30. The processing device of claim 29 further comprising determining the node ID of the destination processing device based upon a set of most significant bits of the destination address of the peripheral bus transaction.

31. The method of claim 29 further comprising choosing to route the peripheral bus transaction according to the primary routing based upon node ID register contents.

32. The method of claim 29 further comprising applying the override routing to cache coherency peripheral bus transactions.

33. The method of claim 29 further comprising applying the override routing to input/output peripheral bus transactions.

34. The method of claim 29 further comprising applying the override routing to both cache coherency peripheral bus transactions and to input/output peripheral bus transactions.

35. The method of claim 34, further comprising applying the primary routing to packet data peripheral bus transactions.